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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

DATE:	March 26, 2003
CLIENT NO.:	M4065.0184
MESSAGE TO:	Examiner Chuong A. Luu
COMPANY:	U.S. Patent and Trademark Office, Art Unit 2825
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PAGES (Including Cover Sheet): 5 **HARD COPY TO FOLLOW:** ☐ YES ☒ NO

Please file the attached Request for Reconsideration in U.S. Patent Application No. 09/594,510. The undersigned certifies that the attached Request for Reconsideration is being transmitted to the U.S. Patent and Trademark Office by facsimile transmission on March 26, 2003.

Mark J. Thronson, Reg. No. 33,082

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Docket No.: M4065.0184/P184
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alan G. Wood, et al

Application No.: 09/594,510 Group Art Unit: 2825

Filed: June 16, 2000 Examiner: C. Luu

For: SEMICONDUCTOR DEVICE PACKAGE AND METHOD

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REQUEST FOR RECONSIDERATION

Box Non-Fee Amendment
Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action dated December 26, 2002 (Paper No. 11), please reconsider the above-identified U.S. Patent application in light of the following remarks:

Claims 1-19 and 35-38 are rejected under 35 USC §103(a) as being unpatentable over Kata in view of Heo. Applicants respectfully request reconsideration. Claim 1 recites the steps of, first, "forming a layered assembly by attaching a wafer to a dielectric layer," second, "testing semiconductor devices in said wafer," and third, "dicing said layered assembly." Kata and Heo fail to suggest the sequence recited in claim 1, even when considered together. Kata (Figs. 8D, 8E, 9A-9C) suggests the semiconductor chips are "diced out one by one from the semiconductor wafer" (col. 7, lines 56-57), then attached to a "carrier film [which] includes organic insulating film" (col. 7, lines 60-61); this carrier film is then "cut...so as to provide the semiconductor device of a chip size" (col.

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8, lines 27-29). Kata fails to disclose or suggest testing, as acknowledged by the Office Action (p. 3).

Heo (Figs. 3d-3g) "test[s]...semiconductor chips in wafer state" (col. 4, lines 16-20), then dices the wafer into chips, and only then attaches "good...chips...to [a] circuit board sheet" (col. 5, lines 20-24), which is then "cut[]...into chip size packages" (col. 3, lines 26-27). The prior art references, even when considered in combination, suggest the sequence of claim 1. The sequence of forming the layered assembly, testing semiconductor devices "in said wafer," and *then* dicing is an important aspect of the claimed invention. Therefore, claim 1 should be allowable over the combined teachings of the cited references. Claims 2-10 depend from independent claim 1 and are believed to be allowable along with claim 1 and for other reasons.

Claim 11 recites "forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to a dielectric layer,...and subsequently, dicing said layered assembly." As with claim 1, Kata and Heo fail to suggest the sequence recited in claim 11, even when considered together. Further, Kata fails to disclose or suggest a "stiff metal layer." Instead, Kata refers only to "wiring layers...formed by processing, such as etching, a metal foil...into desired shapes" (col. 4, lines 16-18; col. 7, lines 60-64). Kata's metal foil etched into wiring would suffer the drawbacks of a package without sufficient stiffness (application, page 2, lines 27-28). The "stiff metal layer" is an important aspect of the invention of claim 11 (application, page 3, lines 24-27). Heo is cited in the Office Action for other features. Therefore, claim 11 should be allowable over the combined teachings of the cited references. Claims 12-18 depend from independent claim 11 and are believed to be allowable along with claim 11 and for other reasons.

Claim 19 recites a "method of...aligning a semiconductor wafer with respect to a dielectric tape," then, "simultaneously dicing said wafer and said dielectric tape." Once again, Kata and Heo fail to suggest the sequence recited in claim 19, even when considered together. Furthermore, both Kata and Heo fail to disclose or suggest the step of aligning.

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Therefore, claim 19 should be allowable over the combined teachings of the cited references.

Claim 35 recites "adhering said wafer to a flexible substrate; connecting said semiconductor devices to respective ball grid arrays...and testing said semiconductor devices through said ball grid arrays." Once again, Kata and Heo fail to suggest the sequence recited in claim 35, even when considered together. Furthermore, Kata fails to disclose or suggest testing and Heo fails to disclose or suggest "testing said semiconductor devices through said ball grid arrays." Rather, Heo (Figs. 3d-3g) "test[s]...semiconductor chips in wafer state" (col. 4, lines 16-20), dices the wafer into chips, attaches "good...chips...to [a] circuit board sheet" (col. 5, lines 20-24), "fus[es]solder balls...as input/output ports" (col. 3, lines 24-25), and finally "cut[s]...the circuit board sheet into chip size packages" (col. 3, lines 26-27). Testing the entire semiconductor device, including the chip and circuit board assembly, through the ball grid arrays is an important aspect of the invention of claim 35. Therefore, claim 35 should be allowable over the combined teachings of the cited references. Claims 36-38 depend from independent claim 35 and are believed to be allowable along with claim 35 and for other reasons.

Claim 20 is rejected under 35 USC §103(a) as being unpatentable over Kata in view of Heo, and further in view of Gaynes. Claim 20 depends from independent claim 19 and should be allowable along with claim 19 and for other reasons.

Claims 21-23 are rejected under 35 USC §103(a) as being unpatentable over Kata in view of Heo, and further in view of Huddleston. Claims 21-23 depend from independent claim 19 and should be allowable along with claim 19 and for other reasons.

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Application No.: 09/594,510 Docket No.: M4065.0184/P184

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: March 26, 2003

Respectfully submitted,

By

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